WHAT IS CLAIMED IS:

1. A twin-cell type semiconductor memory device for storing data in a pair of memory cells as complementary information, wherein the memory cells are arranged at each of word lines at intervals at which bit lines are located.

2. The semiconductor memory device according to claim 1, wherein each of the memory cells includes one transistor and one storage element.

3. The semiconductor memory device according to claim 1, wherein the bit lines are arranged as a folded bit line.

4. The semiconductor memory device according to claim 1, wherein contacts for connecting the bit lines and diffusion layers are arranged along the word lines at the intervals at which the bit lines are located.

5. The semiconductor memory device according to claim 1, wherein one word line not driven is located for every two word lines.

6. The semiconductor memory device according to claim 5, wherein fixed potential is applied to the word line not driven.

7. The semiconductor memory device according to claim 6, wherein the fixed potential is word line reset potential for

resetting the word line.

8. The semiconductor memory device according to claim 6, wherein the fixed potential is power supply potential used in an integrated circuit.

9. The semiconductor memory device according to claim 1, wherein one word line is not located for every two word lines.

10. The semiconductor memory device according to claim 1, wherein the word lines are shunted by a metal wiring.

11. The semiconductor memory device according to claim 10, wherein the metal wirings are formed at intervals not wider than one and a half times an interval between the word lines.

12. The semiconductor memory device according to claim 1, wherein COB structure is formed.

13. The semiconductor memory device according to claim 1, wherein CUB structure is formed.

14. The semiconductor memory device according to claim 3, wherein the pair of bit lines arranged as the folded bit line are formed in the same wiring layer.